Application Note

Thermal Management of Guerrilla RF GaN Devices in the 3×3 mm QFN Package: PCB Thermal Management Guide

AN011

1. Introduction

Guerrilla RF offers a growing family of GaN-on-SiC HEMT devices in an industry-standard 3×3 mm QFN-16 surface mount package. These devices serve applications ranging from 5G cellular infrastructure and radar to electronic warfare, tactical communications, and test instrumentation. Power levels span from a few watts to 30 W saturated output, with operating frequencies from DC to 8 GHz and beyond.

While the 3×3 mm QFN-16 package provides excellent RF performance in a compact footprint, the high-power densities achievable with GaN-on-SiC technology create significant thermal management challenges at the PCB level.

This application note presents four PCB-level thermal management approaches for Guerrilla RF GaN devices in the 3×3 mm QFN-16 package, covering a range of power levels and fabrication constraints. The primary recommendation is an embedded rectangular copper coin (Section 7), which provides a solid copper conduction path through the full PCB thickness and is the preferred solution for devices dissipating more than approximately 6 W. For moderate power levels (3–10 W) where standard PCB processes are preferred, a copper-filled via array (Section 5) offers substantially better thermal performance than conventional hollow vias without requiring special PCB construction. For the highest power densities or precision assemblies mounted to a machined carrier, a thermal pillar integrated into a metal base plate (Section 6) eliminates the PCB laminate from the thermal path entirely. A worked example using the GRF0020 (30 W, DC–7 GHz) is provided in Section 9 to illustrate the thermal analysis methodology.

Method	Power range	Rθ j-hs typical (°C/W)	PCB complexity	Key advantage	Key constraint
Hollow via array (no fill)	< 3 W	~18.7	Standard; no fill specification required	Lowest cost and complexity; no special PCB processing	Very high thermal resistance; not viable above ~3 W dissipation
Copper-filled via array	3–10 W	~1.85	Standard; IPC-4761 Type VII fill spec required	No special PCB construction; lowest cost of four methods	Limited lateral spreading; >10 W requires coin or pillar
Thermal pillar / base plate	Any; > 10 W typical	~0.89	High; requires machined	No laminate in thermal path; lowest	Highest system cost; pillar height

			metal carrier or chassis	Tj scatter in production	tolerance critical
Embedded copper coin	> 6 W	~0.76	Moderate; coin pocket milled and laminated by PCB fab	Large lateral spreading area; best Rθ of PCB-only solutions	Solder void control critical; requires inner PCB layer for slug bonding

Table 1a. Thermal management method comparison. θjb values based on 3×3 mm QFN-16, Rogers 4350B 24.2 mil stack-up, GRF0020 in-package resistances.

2. The 3×3 mm QFN-16 Package

2.1 Package Overview

The 3×3 mm QFN-16 package used across the Guerrilla RF GaN product line features the following thermal-relevant characteristics:

- Body dimensions: 3.0×3.0 mm, 0.8 mm height.
- Lead configuration: leads on two opposing sides only (8 leads per side), with two sides completely free of lead connections.
- Exposed die-attach pad (die flag): 1.7×1.7 mm, centered on the package bottom.
- Die flag area: 2.89 mm². All device heat dissipation flows through this interface.

As noted above, only two of the four sides carry RF signal leads. This is a key enabler for the enhanced thermal management approaches described in Sections 3–7: the two lead-free sides provide clearance for a copper coin to extend beyond the package footprint, and for the through-PCB clearance hole required by the thermal pillar configuration.

2.2 Heat Path

In a properly designed system, the dominant heat path is:

- GaN channel → SiC substrate → die attach → die flag (inside the package).
- Die flag → solder joint → PCB thermal landing pad (package-to-board interface).
- Thermal landing pad → PCB thermal structure (via array, copper coin, or thermal pillar — see Section 3) → TIM (Thermal Interface Material) → heatsink (board-to-system interface).

The secondary path through the mold compound to ambient air is negligible for high-power operation and should not be relied upon for thermal management.

2.3 Thermal Design Thresholds

The heat flux at the die flag interface is the key driver of thermal management approach selection. With a 1.7×1.7 mm die flag (2.89 mm²), heat flux equals P_diss / 2.89 W/mm². Below 1.0 W/mm² (< 3 W) a hollow via array is adequate; from 1.0–3.5 W/mm² (3–10 W) copper-filled vias offer a cost-effective improvement with standard PCB processes; above 2.0 W/mm² (> 6 W) an embedded copper coin is preferred for PCB-only assemblies; a thermal pillar is appropriate at any power level where a machined metal carrier is available. See Table 1 in the Introduction for a full comparison of all four methods and their applicable power ranges.

3. PCB Thermal Management Method Comparison

This section examines the four PCB-level thermal management approaches available for Guerrilla RF GaN devices in the 3×3 mm QFN-16 package: hollow via arrays, copper-filled via arrays, thermal pillar base plates, and embedded copper coins.

3.1 Hollow Via Array Advantages

A standard hollow plated-through via array is the default PCB thermal management approach for QFN packages and serves as the performance baseline in this application note. Each via is a thin-walled copper cylinder with an air or solder-filled interior; only the copper barrel wall conducts heat, giving a very small effective thermal cross-section per via. The hollow via array is viable only for devices dissipating less than approximately 3 W average; above this level one of the three enhanced approaches described in Sections 3.2–3.4 is required. Three fundamental limitations explain this power ceiling:

- Each conventional via is a thin-walled copper cylinder (typically 25–50 µm wall thickness) with an air or solder-filled core, yielding effective thermal conductivity far below that of solid copper.
- Conventional via arrays create multiple series thermal resistances: copper barrel walls, solder or air fill, and interfaces between the via and copper planes on each layer. The resulting PCB-level thermal resistance is approximately 17–18 °C/W for a five-via array on the 24.2 mil Rogers 4350B stack-up—two orders of magnitude worse than the copper coin and 10× worse than a copper-filled via array.
- Typical total channel-to-heatsink thermal resistance is approximately 18.7 °C/W when in-package and TIM terms are included, yielding channel temperatures far above safe operating limits at any meaningful power level.
- Solder wicking during reflow pulls solder away from the die flag interface and into hollow via barrels, creating voids that further degrade thermal performance.

3.2 Copper-Filled Via Advantages

A copper-filled via array (IPC-4761 Type VII) fills each via barrel completely with solid electroplated copper, eliminating the hollow air core that makes conventional vias poor thermal conductors. This produces a via with an effective thermal cross-section 2–3× larger than a conventional plated barrel, yielding substantially lower PCB-level thermal resistance without requiring the specialised coin embedding process. Copper-filled vias are in routine production at most commercial PCB fabricators and represent the lowest-cost path to meaningful thermal improvement over the hollow via baseline. The detailed design guidelines for the copper-filled via approach are covered in Section 5.

3.3 Thermal Pillar Advantages

A thermal pillar is a precision-machined metal post, integral to a metal base plate or chassis, that passes through a clearance hole in the PCB and makes direct contact with the QFN exposed paddle through a thin TIM layer. By routing heat entirely through solid metal — bypassing the PCB laminate completely — the pillar approach achieves the lowest possible junction-to-carrier thermal resistance of any PCB-integrated solution. Its key advantages over the copper coin are:

- No laminate in the thermal path. Rogers 4350B has a through-plane thermal conductivity of only 0.7 W/mK; the pillar bypasses it entirely, so thermal resistance is governed solely by the TIM bond-line and the bulk metal of the carrier.
- Tighter Tj production distribution. Coin-based designs are sensitive to PCB lamination quality and solder void fraction; the pillar's thermal resistance is set by machining tolerances and TIM bond-line thickness, which are both more controlled and more consistent lot-to-lot.

- No coin lamination constraints. The coin requires a 3-layer PCB with a bonding inner copper layer; the pillar places no constraints on PCB layer count or stack-up, making it compatible with any Rogers 4350B construction.
- Integral mechanical and thermal structure. The pillar and base plate are a single machined part, providing a rigid ground reference, a precision heatsink interface, and the thermal path in one component without the complexity of aligning a separate coin, PCB, and heatsink.

The primary trade-off is system cost and mechanical complexity: the pillar requires a machined metal carrier or chassis, making it most appropriate for military, aerospace, and high-reliability commercial assemblies where the board is already mounted to a precision structure. For standard PCB assemblies without a machined carrier, the embedded copper coin (Section 7) remains the preferred solution. The detailed design guidelines for the thermal pillar are covered in Section 6.

3.4 Copper Coin Advantages

An embedded copper coin replaces the via array with a solid copper mass spanning the full PCB thickness. The coin provides a continuous metal path from the device thermal pad to the heatsink interface, eliminating the series resistances inherent in via-based designs.

Parameter	Hollow Via Array (no fill)	Cu-filled Via Array	Thermal Pillar	Copper Coin
Thermal resistance	~17.8 °C/W (5 hollow vias, Cu wall only)	~1.3 °C/W (Cu-filled, 5×5 array)	~0.32 °C/W (TIM only)	< 0.5 °C/W
Heat path	Thin Cu barrel walls through laminate; air interior	Solid Cu barrels through laminate	Paddle → TIM → Cu pillar → base plate	Solid copper mass
Lateral spreading	Negligible; copper barrel walls only	Limited by Rogers 4350B	None in PCB; base plate provides spreading	400 W/mK in copper
Thermal cycle reliability	Good; no fill material to crack or fatigue	Low (solid Cu fill eliminates barrel fatigue)	Excellent; no solder joint in thermal path	2–3× cycle life
Solder wicking risk	High; open barrels wick solder during reflow, increasing voiding	None (IPC-4761 Type VII cap; no open barrel)	None; TIM interface not soldered	None (no vias in coin)

Table 3a. Thermal management method comparison — via array, copper coin, thermal pillar, and hollow via array.

Note: No thermal vias should be placed within the copper coin area. The coin is a solid copper mass; drilling vias into it removes copper and reduces thermal conductivity. Thermal vias are only appropriate in the Rogers 4350B regions outside the coin for supplemental ground connections if needed.

4. Hollow Via Array PCB Design

This section covers the design parameters for a standard hollow plated-through via array, the baseline thermal management approach for the 3×3 mm QFN-16. No special PCB processes are required; the section exists primarily to document the specification and to confirm the 3 W power ceiling before the reader selects one of the enhanced methods in Sections 5–7.

4.1 Via Specification

Hollow vias require no fill or cap specification. The thermal performance is determined entirely by the copper barrel wall cross-section; all other design rules follow standard PCB practice.

Parameter	Value	Notes
IPC fill standard	None required	Standard plated barrel; no fill or cap specification needed
Via drill diameter	0.25–0.30 mm	Aspect ratio ≤8:1; 0.25 mm preferred
Copper wall thickness	25–50 µm	Nominal plating; only the barrel wall conducts heat
Via pitch	0.60–0.75 mm	Wider spacing than copper-filled; reduces solder wicking conduit density
Array count (3×3 mm QFN)	5 vias (cross pattern)	Centre via on die flag centre; four at ±0.4 mm offset
Effective thermal resistance	~17–18 °C/W (5-via array)	Cu barrel wall area only; air interior is negligible conductor

Table 4a. Hollow via array specification for 3×3 mm QFN-16 thermal management.

4.2 Thermal Resistance and Power Limit

For a five-via cross array of 0.25 mm diameter vias with 25 µm copper wall thickness, the effective copper cross-section is 0.088 mm². On the 24.2 mil (0.615 mm) Rogers 4350B stack-up this yields a PCB-level thermal resistance of approximately 17.8 °C/W, and a total channel-to-heatsink resistance of approximately 18.7 °C/W when in-package and TIM terms are included. The full derivation is worked in Sections 9.3–9.4.

This resistance limits the hollow via array to devices dissipating less than approximately 3 W average. Above this threshold, channel temperature at any reasonable heatsink temperature exceeds safe operating limits. One of the enhanced approaches in Sections 5–7 is required.

4.3 Assembly Considerations

The principal assembly risk with hollow vias is solder wicking: open via barrels draw solder paste away from the die flag interface during reflow, increasing void fraction and raising effective thermal resistance above the already-high baseline. The following precautions reduce but do not eliminate this risk:

- Use a cross-hatched stencil aperture (see Section 8.4) with 60–70% paste coverage to allow trapped gas to escape and reduce voiding.

- Do not use via-in-pad without fill. Hollow vias placed directly under the die flag create surface depressions that cause device tilt, poor solder wetting, and accelerated wicking. If via-in-pad placement is required for layout reasons, upgrade to IPC-4761 Type VII copper-filled vias (Section 5).
- Apply X-ray inspection per lot to verify void fraction remains below 25% of the die flag area. Voids exceeding 50% will substantially degrade thermal performance even at sub-3 W dissipation levels.

5. Copper-Filled Via PCB Design

This section provides detailed design guidelines for the copper-filled via array approach introduced in Section 3.2.

5.1 Via Specification and Standards

Specify copper-filled vias to IPC-4761 Type VII (filled and capped) on the PCB fabrication drawing. Type VII requires the via barrel to be completely filled with electroplated copper and both top and bottom surfaces to be planarized and capped with copper overfill. The planarized cap is essential for via-in-pad applications (see Section 8.3) to provide a flat, solderable surface directly over the via. Recommended via dimensions for this application are given in Table 5.

Parameter	Value	Notes
IPC standard	IPC-4761 Type VII	Filled and capped; specify on fab drawing
Via drill diameter	0.20–0.30 mm	Aspect ratio ≤ 8:1 for reliable fill; 0.25 mm preferred
Via pitch	0.45–0.60 mm	Tighter pitch maximises array density; check fab DRC
Array count (3×3 mm QFN)	9–25 (3×3 to 5×5)	Centre array on die paddle; 5×5 recommended for Pd > 6 W
Effective thermal conductivity	390 W/mK (via fill)	Copper fill only; Rogers 4350B between vias has negligible effect on θ

Table 5a. Copper-filled via specification for 3×3 mm QFN-16 thermal management.

5.2 Thermal Resistance Calculation

The thermal resistance through the via array is determined by the total solid copper cross-section, not the gross pad area. For a 5×5 array of 0.25 mm diameter copper-filled vias on the 24.2 mil (0.615 mm) Rogers 4350B stack-up:

$$A_{Cu} = 25 \times \pi(0.125\ \text{mm})^2 = 1.23\ \text{mm}^2$$

$$\theta_{vias} = t / (k_{Cu} \times A_{Cu}) = 0.615\ \text{mm} / (390\times10^{-3}\ \text{W/mm·K} \times 1.23\ \text{mm}^2) \approx 1.28\ °\text{C/W}$$

Adding the in-package resistances (θSiC + θdie-attach + θsolder = 0.57 °C/W from Table 9), the total junction-to-board thermal resistance for a 5×5 copper-filled via array is approximately 1.85 °C/W. This is a 5× improvement over a standard hollow via array and places the copper-filled approach within the power range covered by the embedded copper coin in Table 1, making it a credible option for devices dissipating up to approximately 8–10 W with adequate heatsinking.

5.3 Via-in-Pad and Assembly Considerations

Via-in-pad refers to a layout in which via drill openings fall within the solder pad boundary — here, the 1.6×1.6 mm thermal landing pad under the QFN die flag. Whether the copper-filled array is via-in-pad depends on the array size and pitch. At the tighter end of the Table 5 pitch range (0.45 mm), a 5×5 array spans approximately 1.8×1.8 mm and the outer row of vias falls partly outside the landing pad. At the wider end (0.60 mm) the array spans 2.4×2.4 mm and is entirely outside the pad. A 3×3 array at 0.45 mm pitch spans 0.9×0.9 mm and is fully within the pad. When vias fall within the landing pad boundary, IPC-4761 Type VII fill and cap is mandatory. Without planarization, via barrel openings create surface depressions that wick solder paste downward during reflow, increase voiding, and can tilt the device. The copper-filled and capped via presents a flat, solderable surface flush with the surrounding pad, eliminating these risks. When all vias are outside the landing pad boundary, the Type VII fill specification is still strongly recommended for thermal performance but is not required for solderability. The following assembly notes apply in either case:

- Apply the same cross-hatched stencil aperture pattern described in Section 8.4. Void targets (< 25% area) and X-ray inspection requirements from Section 8.3 remain applicable.
- The copper cap overfill from the plating process typically adds 5–15 µm above the surrounding copper surface. Verify with the PCB fabricator that the cap is within the ENIG or OSP surface finish tolerance so the via sits level with the pad.
- No additional TIM or heatsink interface is needed at the bottom of the via array. Thermal spreading occurs within the PCB bottom copper plane, which then contacts the heatsink through the TIM layer described in Section 8.5. This is simpler mechanically than the coin or pillar approaches.

5.4 Copper-Filled Via Array vs. Other Methods

Copper-filled vias are best suited to applications where power dissipation is moderate (3–10 W), standard PCB fabrication lead times and costs are important constraints, and no machined base plate or heatsink carrier is available. The copper coin is the preferred choice when dissipation exceeds 10 W, when the extended rectangular coin geometry (Section 7.2.3) is needed for lateral spreading, or when via-in-pad fabrication adds unacceptable cost or schedule risk.

6. Thermal Pillar / Base Plate PCB Design

This section provides detailed design guidelines for the thermal pillar / base plate approach introduced in Section 3.3.

6.1 Concept and Configuration

Unlike an embedded copper coin, which is fabricated as part of the PCB, the thermal pillar is a separate precision-machined component that forms an integral feature of the system carrier plate. The pillar passes through a clearance hole routed or drilled through the full PCB thickness. The top face of the pillar sits flush with, or very slightly proud of, the PCB top copper surface. A thin TIM layer (typically indium sheet at 50–75 µm bond-line thickness) is applied between the pillar top face and the QFN exposed paddle. The result is a thermal path that consists of: GaN channel → SiC substrate → die attach → exposed paddle → TIM → Cu pillar → base plate → heatsink. The PCB laminate plays no role in heat conduction. The pillar is most appropriate where the PCB is already mounted to a machined chassis or cold plate; for standard PCB-only assemblies, the embedded copper coin (Section 7) is the preferred solution.

6.2 Thermal Resistance Analysis

Because the laminate is bypassed entirely, the thermal resistance from exposed paddle to base plate is governed only by the TIM bond-line. Using indium sheet (k ≈ 80 W/mK, BLT = 75 µm) over the 2.89 mm² die paddle area:

θTIM = BLT / (k×A) = 0.075 mm / (80 W/mK × 2.89 mm²) ≈ 0.32 °C/W

Adding the in-package resistances from Table 9 (θSiC = 0.27 °C/W, θdie-attach = 0.15 °C/W, θsolder = 0.15 °C/W), the total channel-to-base-plate thermal resistance is approximately 0.89 °C/W. This is 0.13 °C/W higher than the copper coin result of 0.76 °C/W. The difference arises because the coin spreads heat laterally before the TIM interface, increasing the effective TIM contact area from 2.89 mm² (die paddle only) to 10.2 mm² (full coin face), which substantially reduces TIM resistance. The pillar's advantage is not lower absolute thermal resistance but rather tighter Tj distribution across production boards, where coin-based designs are sensitive to solder void fraction and PCB lamination quality.

6.3 Pillar Geometry and Mechanical Tolerances

The pillar top face must be coplanar with the PCB top copper surface within a tight tolerance to ensure a uniform TIM bond-line. The following guidelines apply to the 3×3 mm QFN-16 on the 24.2 mil Rogers 4350B stack-up described in Section 7.3.

Parameter	Value	Notes
Pillar material	OFC Cu (C101) or CuW	CuW reduces CTE mismatch to Rogers laminate
Pillar top face height	PCB thickness ± 25 µm	Flush with top Cu surface; controls TIM BLT
PCB clearance hole	Pillar OD + 0.1–0.2 mm	Accommodates CTE mismatch; maintain keepout from signal pads
TIM material	Indium sheet, 50–75 µm	k ≈ 80 W/mK; clamping force required
Pillar surface finish	Ni/Au (ENIG) or bare Cu + OSP	Flatness Ra < 0.4 µm to minimise TIM BLT variation
RF grounding	Via stitching to PCB ground	Pillar must not float electrically; tie to ground at PCB perimeter

Table 6a. Thermal pillar geometry and tolerance guidelines.

7. Copper Coin PCB Design

7.1 Exploiting the Two-Sided Lead Configuration

The GRF0020 3×3 mm QFN-16 package uses leads on only two opposing sides. This configuration leaves two sides of the package completely free, creating space for the copper coin to extend as a rectangle far beyond the package boundary. This is a fundamental advantage over other QFN devices where leads on all four sides are used for connections and constrain the coin to approximately the die flag footprint.

By extending the coin along the lead-free axis, the designer gains two benefits: a much larger conduction cross-section for vertical heat transfer, and lateral heat spreading within the coin that reduces peak heat flux at the TIM-to-heatsink interface.

7.2 Coin Geometry

7.2.1 Recommended Dimensions

Parameter	Dimension	Notes
Die flag (all 3×3 QFN-16)	1.7 × 1.7 mm	Fixed by package design
Coin width (constrained axis)	1.7 mm	Matches die flag width; maintain ≥ 0.2 mm clearance to lead pads
Coin length (unconstrained axis)	6.0 mm	Suitable for moderate-to-high power dissipation
Coin thickness	Full PCB thickness	24.2 mil (0.615 mm), see Table 4 stack-up
PCB thermal landing pad	1.6 × 1.6 mm	Slightly undersized vs. die flag to prevent solder bridging
Lead-to-coin clearance	≥ 0.2 mm	From nearest lead landing pad edge, verify against Gerber files

Table 7a. Recommended copper coin dimensions.

7.2.2 Constrained Axis (Between Lead Rows)

On the 3.0 mm package body, the inner edges of the lead rows sit approximately 0.8–1.0 mm from the package center on each side. The coin width of 1.7 mm matches the die flag width exactly, providing the maximum coin area possible on the constrained axis while maintaining adequate clearance to the lead landing pads. The exact clearance should be confirmed against the specific device datasheet and Gerber files before finalizing the layout.

7.2.3 Unconstrained Axis (Lead-Free Sides)

The coin extends freely along the lead-free axis. The 6.0 mm coin length (extending approximately 2.5 mm beyond each lead-free edge of the 3.0 mm package body) provides a good balance of thermal performance and board space for moderate-to-high power applications. The coin must be symmetric about the package center in both axes to avoid uneven thermal gradients across the die.

7.3 PCB Stack-Up

The recommended PCB construction uses Rogers 4350B laminate with three copper layers and an embedded copper coin. The inner copper layer is required by PCB fabricators as a mechanical bonding surface for the copper slug during lamination. Without an inner copper layer, the slug has insufficient adhesion to the surrounding prepreg and can delaminate under thermal cycling.

Layer	Thickness	Material	Notes
Top copper	1.4 mil (35 µm)	Copper (1 oz)	RF traces, ground pours, bias network
Dielectric 1	10 mil (0.254 mm)	Rogers 4350B	Dk 3.66, tan d 0.004 at 10 GHz
Inner copper	1.4 mil (35 µm)	Copper (1 oz)	Solid pour for slug bonding; void under all RF traces
Dielectric 2	10 mil (0.254 mm)	Rogers 4350B	Lower core laminate
Bottom copper	1.4 mil (35 µm)	Copper (1 oz)	Ground plane; coin bottom face flush with this surface
Total	**24.2 mil (0.615 mm)**	**—**	**Full PCB thickness = copper coin thickness**

Table 7b. PCB layer stack-up.

Inner copper (1.4 mil / 1 oz): Continuous copper pour across the board footprint, with clearance voids beneath all RF traces. The surrounding copper provides the bonding surface for the coin slug during PCB lamination and contributes to the DC and RF ground network. Voids under RF traces prevent the inner layer from perturbing the characteristic impedance of the top-layer transmission lines.

Inner layer void rule: Remove all inner-layer copper beneath any top-layer RF trace. The void width should extend at least 3× the trace width beyond each trace edge to ensure the effective dielectric seen by the RF trace is determined solely by the top dielectric layer (10 mil Rogers 4350B). Inner copper is a solid pour everywhere else.

Note: The copper coin slug spans the full 24.2 mil PCB thickness and is inserted into a milled pocket in the Rogers 4350B stack before final lamination. The inner copper layer on the pocket walls bonds to the coin perimeter during lamination, providing mechanical retention. Coordinate with the PCB fabricator regarding pocket tolerances and the lamination cycle to ensure complete bonding and acceptable coin flatness after cure.

8. Solder Interface, Assembly, and Manufacturing

8.1 The Critical Interface

The solder joint between the device die flag and the PCB thermal landing pad is the thermal bottleneck common to all four thermal management approaches. The 1.7×1.7 mm die flag contact area (2.89 mm²) carries all dissipated power regardless of whether it lands on a copper coin, a copper-filled via array, or the top of a thermal pillar. The shared assembly guidelines in Sections 8.2–8.5 apply to all four methods. Method-specific fabrication and assembly notes are given in Sections 8.6 (RF grounding), 8.7 (hollow via array), 8.8 (copper-filled via array), 8.9 (thermal pillar), and 8.10 (copper coin).

8.2 Solder Material

Gold-tin (AuSn) eutectic solder is preferred for its high thermal conductivity (~57 W/mK) and ability to accommodate CTE mismatch. Standard SAC305 lead-free solder is acceptable for applications where AuSn is not required; its thermal conductivity (~33 W/mK for void-free joints) is lower than AuSn and it is more prone to voiding, both of which increase the effective solder joint thermal resistance.

8.3 Void Control

Solder voiding is the single largest risk to thermal performance:

- Target: < 25% void area under the die flag.
- Maximum acceptable: < 50%. Beyond 50%, thermal resistance increases sharply.
- X-ray inspection is recommended for production quality verification. Voids larger than 25% of the total pad area or any single void larger than 15% should be flagged.

8.4 Stencil Design

Use a cross-hatched stencil aperture pattern for the 1.7×1.7 mm thermal landing pad area. A 4-window or 9-window grid within the aperture, achieving approximately 60–70% paste coverage, allows trapped gases to escape during reflow and substantially reduces voiding compared to a single large aperture.

- Recommended stencil thickness: 0.125 mm (5 mil) for devices with 0.5 mm lead pitch.
- Use laser-cut stainless-steel stencils with electro-polished trapezoidal walls for best paste release.
- The stencil aperture for the lead pads should be 1:1 to the PCB pad size.

8.5 Heatsink Interface (TIM)

The bottom face of the copper coin interfaces directly with the system heatsink through a thermal interface material. Recommended options, in order of thermal performance:

TIM Type	Thickness	k (W/mK)	Clamping	Coverage
Indium sheet	50–100 µm	~80	Required	Full area
Graphite film	50–100 µm	10–15 (thru)	Required	Full area
Thermal grease	25–50 µm	3–8	Moderate	≥ 80%

Table 8a. Thermal Interface Material options.

8.6 RF Grounding

The extended copper coin acts as a ground reference for RF traces routed over it. This can be beneficial for controlled impedance if the coin is properly connected to the ground reference on all copper layers. However, if the coin is poorly grounded or electrically floating, it may behave as a parasitic resonator at RF frequencies. Ensure solid ground connections at multiple points along the coin perimeter, particularly at the edges nearest the device leads.

8.7 Hollow Via Array — Assembly Notes

The hollow via array uses the same standard QFN reflow process as any other SMT assembly. The only method-specific concern is solder wicking into the open via barrels, which reduces solder volume at the die flag interface and increases void fraction. The following steps minimise this risk:

- Stencil aperture: use a cross-hatched pattern over the die flag pad with 60–70% open area (consistent with the guidance in Section 8.4). The bridges prevent bridging while the open areas provide flux outgassing paths that reduce voiding.
- Solder paste volume: do not over-print. Excess paste accelerates wicking. A 5 mil stencil with 65% aperture coverage is a suitable starting point; adjust based on X-ray results.
- Reflow profile: use a slow ramp (≤ 1.5 °C/s) through the liquidus region to allow flux outgassing before the solder wets the via barrels. A rapid ramp increases the pressure differential driving wicking.

- Post-reflow inspection: X-ray inspect per lot. Void fraction at the die flag interface must remain below 25% of the 2.89 mm² flag area. Because the hollow via array provides no thermal redundancy, apply tighter rejection criteria than for copper-filled or coin designs.
- No TIM at the via exit side: no heatsink interface preparation is required at the bottom of the board. Heat spreads through the bottom copper plane and exits to the heatsink through the standard TIM layer described in Section 8.5.

8.8 Copper-Filled Via Array — Assembly Notes

The copper-filled via array requires no special PCB assembly steps beyond the standard copper coin process described in Sections 8.1–8.4. The IPC-4761 Type VII filled and capped via presents a flat, solderable surface identical to the surrounding pad, so the stencil aperture, solder paste volume, reflow profile, and void inspection criteria from Sections 8.3 and 8.4 apply without modification. No TIM or heatsink interface work is required at the via side of the board; heat spreading occurs through the bottom copper plane and is carried to the heatsink via the standard TIM layer described in Section 8.5.

8.9 Thermal Pillar / Base Plate — Assembly Notes

Assembly of the thermal pillar configuration differs from the copper coin approach in that the PCB is mounted to the machined base plate before device placement rather than after. The recommended assembly sequence is: (1) verify pillar top-face height flush to PCB top copper within ±25 µm; (2) apply indium TIM sheet to the pillar top face; (3) place and reflow the QFN using standard SAC305 or AuSn solder paste and the profile from Section 8.2; (4) inspect solder joints and void fraction per Section 8.3; (5) secure PCB to base plate with fasteners to the specified clamping torque. The clamping force is critical — it controls the TIM bond-line thickness and therefore the thermal resistance. Refer to the TIM manufacturer's data sheet for the recommended clamping pressure (typically 50–200 psi for indium sheet).

8.10 Copper Coin Fabrication and PCB Assembly Notes

Key manufacturing requirements for the embedded coin:

- Coin material: solid oxygen-free copper (C101 or C110), 400 W/mK thermal conductivity.
- Coin dimensions: 1.7 mm wide × 6.0 mm long × 24.2 mil (0.615 mm) thick, matching the full PCB thickness.
- Surface treatment: brown-oxide treatment before lamination to ensure adhesion between the coin perimeter and surrounding prepreg.
- Embedding accuracy: ±50 µm positional tolerance, verified with automated optical inspection.
- Flatness control: critical for the elongated rectangular geometry. Engage the PCB fabricator early to manage warpage from CTE mismatch between copper and Rogers 4350B during lamination.
- Surface finish: Ni/Au (ENIG) or OSP on both top face (for solder wetting) and bottom face (for TIM interface).

9. Worked Example: GRF0020 — All Four Methods

This section demonstrates the thermal analysis methodology for all four PCB-level thermal management approaches using the GRF0020 as a representative device. Sections 9.1 and 9.2 establish the operating conditions and power dissipation estimate common to all methods. Sections 9.3–9.4 work through the hollow via array baseline, 9.5–9.6 the copper-filled via array, 9.7–9.8 the thermal pillar, and 9.9–9.10 the copper coin. Section 9.11 summarises all four results side by side. The same methodology applies to any Guerrilla RF GaN device in the 3×3 mm QFN-16 package; substitute the appropriate power dissipation from the device datasheet.

9.1 GRF0020 Operating Conditions

Parameter	Value	Condition
Frequency range	DC – 7.0 GHz	—
Saturated output power	30 W (45 dBm)	VDD = 50 V
Saturated drain efficiency	48%	50 V, 3 GHz
Power gain	16 dB	50 V, 3 GHz

Table 9a. GRF0020 key specifications.

9.2 Power Dissipation Estimate

At the PSAT operating point with 50 V drain supply and 48% drain efficiency:

$P_{DC} = P_{OUT} / \eta_{drain} = 30\ W / 0.48 = 62.5\ W$

$P_{diss} = P_{DC} - P_{OUT} = 62.5 - 30 = 32.5\ W$

Note: This represents absolute worst-case CW saturated operation; average dissipation is lower in backed-off or pulsed modes.

The resulting heat flux at the die flag:

$q = P_{diss} / A_{flag} = 32.5 / 2.89 = 11.2\ W/mm^2$

This is well above the ~2 W/mm² threshold where a copper coin is mandatory.

9.3 Hollow Via Array (No Fill) — Thermal Resistance Stack

Using five standard (hollow) plated-through vias, 0.25 mm drill diameter and 25 µm copper wall thickness, on the same 24.2 mil Rogers 4350B PCB with indium TIM. The hollow via interior is air; only the copper barrel wall conducts heat, giving a copper cross-section of 0.088 mm² for five vias.

$A_{Cu} = 5 \times \pi(0.125^2 - 0.100^2)\ mm^2 = 0.088\ mm^2$

$\theta_{vias} = 0.615\ mm / (390 \times 10^{-3}\ W/mm \cdot K \times 0.088\ mm^2) \approx 17.8\ °C/W$

Element	Thickness	K (W/mK)	Area (mm²)	θ (°C/W)	Notes
SiC substrate	0.10 mm	370	~1.0	0.27	In-package
Die attach	0.025 mm	57	2.89	0.15	In-package
Solder joint	0.025 mm	57	2.89	0.15	Bottleneck; open vias increase wicking risk
Hollow via array (5 vias)	0.615 mm	—	0.088 (Cu wall)	17.8	Cu barrel wall area only; air interior negligible conductor
TIM (indium)	0.075 mm	80	~2.89	0.32	Die paddle area only; no lateral spreading through hollow vias

Table 9b. Thermal resistance stack — GRF0020, 5 hollow (unfilled) vias, 24.2 mil Rogers 4350B.

9.4 Hollow Via Array (No Fill) — Channel Temperature

Total thermal resistance from channel to heatsink:

$\theta_{total} \approx 0.27 + 0.15 + 0.15 + 17.8 + 0.32 = 18.7$ °C/W

For worst-case CW saturated operation (32.5 W, 65 °C heatsink):

$T_{channel} = 65 + (32.5 \times 18.7) = 673$ °C

This far exceeds the maximum rated channel temperature of 200–225 °C; the GRF0020 would fail immediately under these conditions. The maximum permissible dissipation for a junction temperature of 150 °C (a conservative reliability target) is approximately 4.5 W, confirming that the hollow via array is appropriate only for devices operating well below 5 W average dissipation.

9.5 Copper-Filled Via Array — Thermal Resistance Stack

Using a 5×5 array of 0.25 mm copper-filled vias (IPC-4761 Type VII) on the same 24.2 mil Rogers 4350B PCB with indium TIM between the bottom copper plane and the heatsink. The same in-package resistances apply; only the PCB-level path changes.

Element	Thickness	K (W/mK)	Area (mm²)	θ (°C/W)	Notes
SiC substrate	0.10 mm	370	~1.0	0.27	In-package
Die attach	0.025 mm	57	2.89	0.15	In-package
Solder joint	0.025 mm	57	2.89	0.15	Bottleneck
Cu-filled via array	0.615 mm	390	1.23	1.28	5×5 Cu-filled vias; 1.23 mm² Cu
TIM (indium)	0.075 mm	80	~6.0	0.16	Spreading in bottom Cu plane

Table 9c. Thermal resistance stack — GRF0020, 5×5 Cu-filled via array, 24.2 mil Rogers 4350B.

9.6 Copper-Filled Via Array — Channel Temperature

Total thermal resistance from channel to heatsink:

$\theta_{total} \approx 0.27 + 0.15 + 0.15 + 1.28 + 0.16 = 2.01$ °C/W

For worst-case CW saturated operation (32.5 W, 65 °C heatsink):

$T_{channel} = 65 + (32.5 \times 2.01) = 130.3$ °C

At 130 °C the channel is below the GaN-on-SiC maximum (200–225 °C), but the margin is insufficient for a 30 W device under demanding CW conditions. The copper-filled via array is appropriate for the GRF0020 only at backed-off or pulsed operation where average P_{diss} is well below 32.5 W. For full CW saturated operation the copper coin or thermal pillar is required.

9.7 Thermal Pillar — Thermal Resistance Stack

Using an OFC copper pillar with indium TIM directly between pillar top face and QFN exposed paddle. The PCB laminate is not in the thermal path; only four elements contribute:

Element	Thickness	K (W/mK)	Area (mm²)	θ (°C/W)	Notes
SiC substrate	0.10 mm	370	~1.0	0.27	In-package
Die attach	0.025 mm	57	2.89	0.15	In-package
Solder joint	0.025 mm	57	2.89	0.15	Bottleneck
TIM (indium)	0.075 mm	80	2.89	0.32	Sole PCB-level resistance; paddle direct

Table 9d. Thermal resistance stack — GRF0020, thermal pillar / metal base plate.

9.8 Thermal Pillar — Channel Temperature

Total thermal resistance from channel to base plate:

θ_total ≈ 0.27 + 0.15 + 0.15 + 0.32 = 0.89 °C/W

For worst-case CW saturated operation (32.5 W, 65 °C base plate):

T_channel = 65 + (32.5 × 0.89) = 93.9 °C

At 93.9 °C the channel temperature is well within the safe GaN-on-SiC operating region with over 100 °C margin. The slightly higher value compared to the copper coin (0.89 vs. 0.76 °C/W) reflects the smaller TIM contact area at the die paddle (2.89 mm²) versus the full coin face (10.2 mm²); the coin benefits from additional lateral spreading before the heatsink interface. In practice the 4.2 °C difference at full power is modest and the pillar offers compensating advantages in Tj uniformity and repeatability.

9.9 Copper Coin — Thermal Resistance Stack

Using the recommended 1.7×6.0 mm copper coin on the 24.2 mil (0.615 mm) three-copper-layer Rogers 4350B PCB with indium TIM:

Element	Thickness	K (W/mK)	Area (mm²)	θ (°C/W)	Notes
SiC substrate	0.10 mm	370	~1.0	0.27	In-package
Die attach	0.025 mm	57	2.89	0.15	In-package
Solder joint	0.025 mm	57	2.89	0.15	Bottleneck
Copper coin	0.615 mm	400	2.89 → 13.6	0.12	1.7×6.0 mm; 24.2 mil PCB thickness
TIM (indium)	0.075 mm	80	~13.6	0.07	Full coin area

Table 9e. Thermal resistance stack for GRF0020 with 1.7×6.0 mm copper coin on 24.2 mil Rogers 4350B PCB.

9.10 Copper Coin — Channel Temperature

Total thermal resistance from channel to heatsink:

θ_total ≈ 0.27 + 0.15 + 0.15 + 0.12 + 0.07 = 0.76 °C/W

For worst-case CW saturated operation (32.5 W dissipation) with a heatsink temperature of 65 °C:

T_channel = 65 + (32.5 × 0.76) = 89.7 °C

This is well within the safe operating region for GaN-on-SiC devices, which typically have maximum channel temperature ratings of 200–225 °C for long-term reliability (> 1 million hours MTTF). The slight increase in thermal resistance compared to a thinner board (0.76 vs. 0.74 °C/W) is the unavoidable consequence of the additional PCB thickness introduced by the inner copper layer; the effect on junction temperature is negligible.

9.11 Method Comparison Summary

The four results for the GRF0020 under worst-case CW conditions (32.5 W, 65 °C heatsink/base plate) are summarized below.

Method	Rθ j-hs (°C/W)	T_channel (°C)	Assessment at 32.5 W CW
Hollow via array (5×, no fill)	18.7	673 (Not viable)	Far exceeds Tj,max at any significant power; viable only below ~5 W average dissipation
Copper-filled via array (5×5)	2.01	130 (Marginal)	Marginal at full CW; adequate at backed-off/pulsed
Thermal pillar / base plate	0.89	93.9 (OK)	Adequate; >105 °C margin to Tj,max
Embedded copper coin (1.7×6.0 mm)	0.76	89.7 (OK)	Adequate; >110 °C margin to Tj,max

Table 9f. GRF0020 channel temperature summary — all four methods. 32.5 W CW, 65 °C heatsink/base plate.

9.12 Adapting This Analysis to Other Devices

To apply this methodology to other Guerrilla RF GaN devices in the 3×3 mm QFN-16 package:

- Determine the device power dissipation at the intended operating point from the datasheet: P_diss = P_DC – P_OUT.
- Calculate heat flux: q = P_diss / 2.89 mm². Use Table 1 to select the appropriate thermal management approach: below ~1.0 W/mm² a standard hollow via array is adequate; above ~2.0 W/mm² an embedded copper coin or thermal pillar is required.
- Apply the appropriate thermal resistance stack (Tables 9, 10a, 10b, or 10c), adjusting only the P_diss value in the temperature calculation.
- Verify that T_channel remains below the device maximum rated channel temperature with adequate margin. **Note:** The in-package thermal resistances (θ_SiC and θ_die_attach) are consistent across all devices in this package family. The solder, coin, and TIM resistances are determined by the PCB design and are device-independent. Only the power dissipation value changes between devices.

10. Design Checklist

The following checklist summarizes the key design parameters for implementing the copper coin thermal management approach. Parameters specific to the hollow via, copper-filled via, or thermal pillar approaches are noted where they differ.

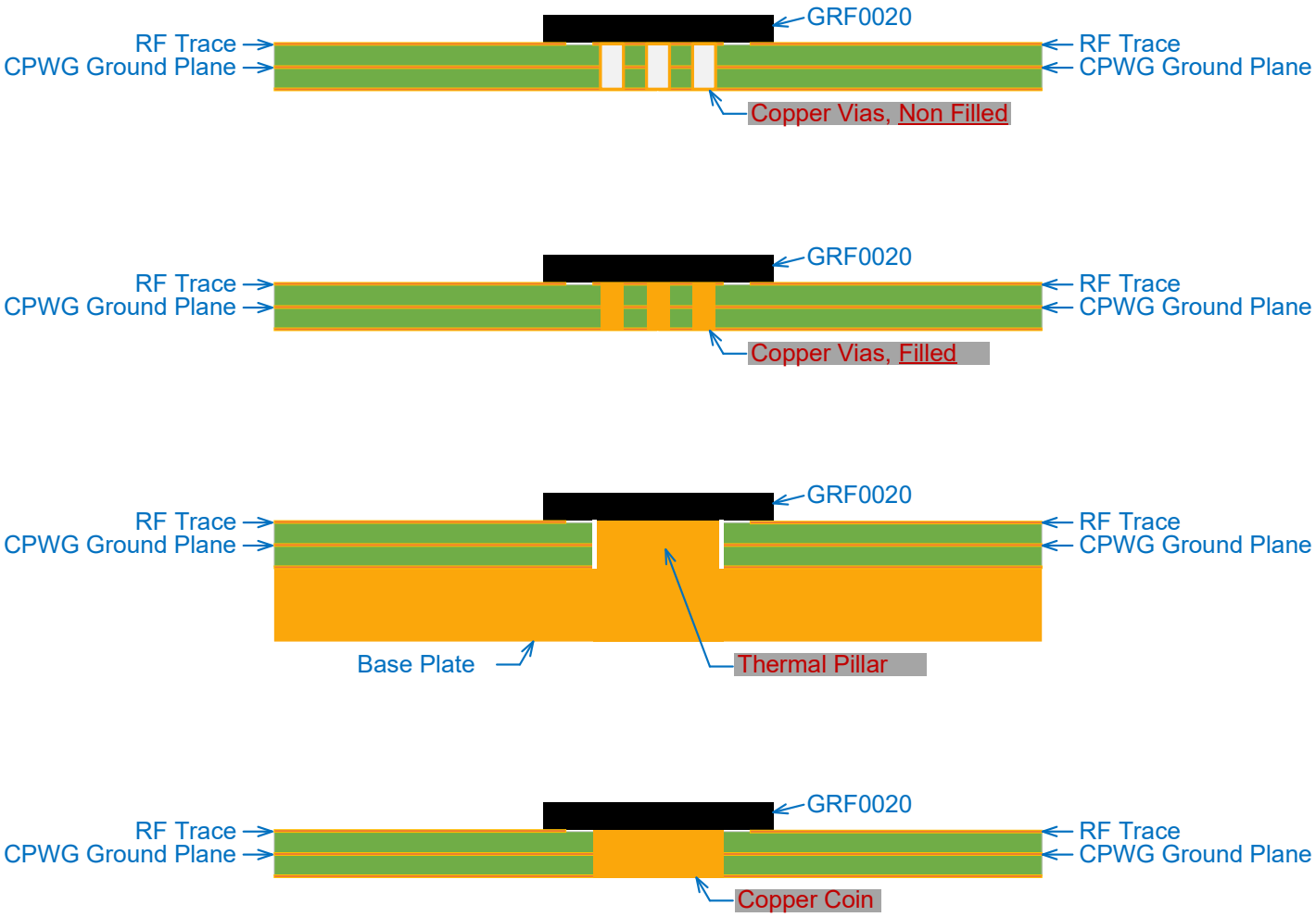
Parameter	Recommendation	Priority
PCB material	Rogers 4350B	Required
PCB layer count	3 copper layers (top / inner / bottom)	Required
Top copper weight	1.4 mil (1 oz / 35 µm)	Required
Dielectric 1 thickness	10 mil Rogers 4350B	Required
Inner copper weight	1.4 mil (1 oz / 35 µm)	Required
Inner copper void rule	No copper under RF traces; solid pour elsewhere	Required
Dielectric 2 thickness	10 mil Rogers 4350B	Required
Bottom copper weight	1.4 mil (1 oz / 35 µm)	Required
Total PCB thickness	24.2 mil (0.615 mm)	Required
Copper coin width	1.7 mm	Required
Copper coin length	6.0 mm	Required
Coin material	Solid OFC copper (C101/C110)	Required
Coin centering	Symmetric on die flag center	Required
Thermal landing pad	1.6 × 1.6 mm	Required
Solder void target	< 25%	Required
Solder void maximum	< 50%	Required
Stencil pattern	Cross-hatched, 0.125 mm thick	Recommended
Lead-to-coin clearance	≥ 0.2 mm	Required
TIM to heatsink	Indium sheet, 50–100 µm	Recommended
Coin surface finish	Ni/Au (ENIG) or OSP	Required
RF ground connection	Solid tie, multiple perimeter points	Required
Coin embedding accuracy	±50 µm	Required
X-ray solder inspection	Per production lot	Recommended

Table 10a. Complete design checklist.

11. PCB Details

3x3 mm GaN package on PCB: Thermal Management Options

(Cross-Section, End View)



12. Conclusion

Guerrilla RF GaN-on-SiC HEMTs in the 3×3 mm QFN-16 package deliver exceptional RF performance at power levels that demand careful thermal management. The document covers four methods in order of increasing thermal performance and fabrication complexity: hollow via array (baseline, ≤ 3 W), copper-filled via array (3–10 W, standard PCB processes), thermal pillar (any power level with a machined carrier), and embedded copper coin (≥ 6 W, PCB-only assemblies). For most high-power applications the copper coin is the recommended solution, exploiting the two-sided lead configuration to embed an extended rectangular copper mass that provides a 24× reduction in PCB-level thermal resistance compared to a hollow via baseline.

With a 1.7×6.0 mm copper coin and indium TIM on the 24.2 mil Rogers 4350B stack-up, the channel-to-heatsink thermal resistance is 0.76 °C/W, yielding a GRF0020 channel temperature of 89.7 °C under worst-case CW conditions — well within the GaN-on-SiC safe operating region with over 110 °C margin to Tj,max.

The critical success factor is solder joint quality at the 1.7×1.7 mm die flag interface. Designers should invest in proper stencil design, reflow profile optimization, and X-ray inspection to ensure void levels remain below 25%.

For additional technical support on implementing this thermal management approach with any Guerrilla RF GaN device, contact Guerrilla RF applications engineering at support@guerrilla-rf.com.

Revision History

Rev	Date	Description
1.0	May 20, 2026	Initial release. v1.0